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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,956	07/13/2000	Kumi Miyachi	1248-0509P	3629

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EXAMINER
DECADY, ALBERT

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/615,956	Applicant(s) MIYACHI ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3,4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims **1 to 7** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No: 11-318485, filed on 11/09/99.

Information Disclosure Statement

3. The reference listed in the information disclosure statement submitted on 07/13/00 and 05/21/01 has been considered by the examiner (see attached PTO-1449).

Drawings

4. The drawings are objected to because of the problems addressed in the attached PTO-948. Correction is required.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1 and 2** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Brown et al (U.S. PN: 5,627,842).

As per claims **1,** Brown et al. disclose a semiconductor device comprising plurality of chips integrally sealed (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, edge connector coupled to the input TDI and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, edge connector coupled to the output TDO), a control signal input terminals for receiving a test control signals (see fig. 2, edge connector coupled to the inputs TMS and TCK) whereby the test signal inputted transferred through the plurality of chips (see fig. 2, "input TDI" and col. 4, lines 3-27) and the test control signals inputted being individually supplied to each of said plurality of chips (see fig. 2, "the inputs of TCK and TMS coupled to each of the chips).

As per claim **2,** Brown et al disclose all subject matter claimed in claim 1 including plurality of chips connected to each other through test output terminal (see col. 4, lines 3-27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **3-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (U.S. PN: 5,627,842)

As per claim **3,** Brown et al. disclose a semiconductor device comprising plurality of chips integrally sealed (see figure 2 and col. 3, lines 49-55), a test signal input terminal

for receiving a test signal (see fig. 2, "input TDI" and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, "output TDO"), a control signal input terminals for receiving a test control signals (see fig. 2, inputs TMS and TCK), whereby the test signal inputted to one of the plurality of chips and transferred through the other chips (see fig. 2, "input TDI" and col. 4, lines 3-27) and the test control signals inputted being individually supplied to each of the plurality of chips (see fig. 2, the inputs of TCK and TMS coupled to each of the chips).
Brown et al did not explicitly teach a single (only one of the) chip connected to the test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips. However, Brown et al. teach mechanics of testing and capable of transferring data between on–chip logic side and the pin by which the chip is connected to the rest of the system (other chips) (see col. 4, lines 28-45) which Brown et al's techniques of transferring data is similar to the applicants method. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to use the techniques of transferring test data through a single chip connected to the input/output test terminals. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to maximize the system's testing performance.

As per claim **4,** Brown et al disclose all subject matter claimed in claim 3 including a chip that includes a controller (TAP controller) for controlling an input/output interface of the test signal (see col. Fig. 4, "TAP controller").

As per claim **5,** Brown et al. disclose a semiconductor device in which a plurality of chips are sealed (see fig. 2) comprising a test registers providing between core logic

and the chips (see fig. 2, "the small squares surround the core logics" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input of a device (see fig. 2, edge connector coupled to the input of TDI), a test data output of a device (see fig. 2, edge connector coupled to the output of TDO) and the said test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the line that connects the four IC's and col. 4, lines 3-27). Brown et al did not explicitly teach a single (only one of the) chip connected to the said test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips. However, Brown et al. teach mechanics of testing and capable of transferring data between on–chip logic side and the pin by which the chip is connected to the rest of the system (other chips) (see col. 4, lines 28-45) which Brown's technique is similar to the applicant's method. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to use the techniques of transferring test data through a single chip connected to the input/output test terminals. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to maximize the system's testing performance.

As per claim **6,** Brown et al disclose a semiconductor device in which plurality of chips sealed (see fig. 2) comprising a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of

TDI), a test data output (see fig. 2, edge connector coupled to the output of TDO), a test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the lines that connect the four IC's and col. 4, lines 3-27). It is unclear whether Brown et al teach a test data device. However, Brown et al teach circuit boards loaded with standard – compliant devices connected together into test rings by local test busses accessible at the edge connectors known entities for down-steam manufacturers and their test engineers (see col. 3, lines 40-42). Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include a test data device. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to because such test data device in order to test or check responses to both valid and erroneous inputs.

As in claim 7, Brown et al. disclose a semiconductor device in which plurality of chips sealed (see fig. 2) comprising a test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the lines that connect the four IC's and col. 4, lines 3-27), a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI) and test data output (see fig. 2, edge connector coupled to the output of TDO). Brown et al did not explicitly teach a single (only one of the) chip connected to the said test signal input terminal and test result output terminal whereby the test signal is transferred to the other

chips. However, Brown et al. teach mechanics of testing and capable of transferring data between on–chip logic side and the pin by which the chip is connected to the rest of the system (including other chips (see col. 4, lines 28-45) which Brown's techniques of transferring data is similar to the applicants method. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to use the techniques of transferring test data through a single chip connected to the input/output test terminals. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to maximize the system's testing performance. As for test data relay input/output is common knowledge for most of IC testing systems. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made use test data relays. This modification would have been obvious because a person having ordinary skill in the art would have been motivated because data relays enable two network systems to use similar functions and different protocols which results in storing and forwarding services rather than a real-time service.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,00,051 Nadeau-Dostie et al

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

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